REMARKS

The Examiner objected to the preamble of Claims 15 and 16. The Examiner rejected Claims 1-28 under 35 U.S.C. § 102(b) as being anticipated by Duncan, Patent Number 6,170,439. Such objections and rejections are noted.

Claims 15, 16, 17, and 20 have been amended. Applicant respectfully submits that Claims 1-28 are allowable.

Claims with Objections

The Examiner objected to the preamble of Claims 15 and 16. As suggested by the Examiner, Claim 15 has been amended to state "The process of Claim 14." Claim 16 has been amended to state "The process of Claim 14." Accordingly, Applicants respectfully submit that the objection to Claims 15 and 16 have been overcome.

Rejection Under 35 U.S.C. § 102(b)

Addressing the Examiner's rejection of Claims 1-28 under 35 U.S.C. § 102(b), Applicant respectfully suggests that Duncan does not anticipate the claims of the present invention. Section 2131 of the Manual of Patent Examining Procedure describes the basis for anticipation under 35 U.S.C. § 102(b). "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990).

The Duncan Reference

Duncan discloses a device for receiving a stimulation signal to be applied to an animal. In describing the operation of one embodiment of the apparatus illustrated in Figure 2, Duncan states:

> The digital output **21** of demodulator representing the stimulus code selected by push-button switches **13** of transmitter **11** then is translated by a microprocessor **22** into one of six possible stimulus level selection signals **23**.

All of the stimulus level selection signals **23** produced by microprocessor **22** have the same pulse width. Intensity selector switch **12** provides six settings for selecting one of six available intensity levels.

The stimulus level selection signal **23** produced by microprocessor **22** is applied to a corresponding input of a pulse generator state machine **24**. State machine **24** operates on the constant-width stimulus level selection signals **23** produced by microprocessor **22** to produce a drive signal **25** consisting of drive pulses the widths of which are determined by which of the six available stimulus level selection signals **23** is applied to pulse generator circuit **24**. The drive pulses are applied to the control electrode of the switch transistor **30** connected to primary winding **31A** of a pulse transformer **31**. The peak-to-peak voltage produced between a pair of electrodes **33** and **34** connected to the secondary winding terminals, respectively, of the pulse transformer **30** corresponds to the pulse width of the drive pulses, and hence to the stimulus level selected by push-button switches **13** of the remote transmitter **11**.

Duncan, Col. 4, line 63, to Col. 5, line 19 (emphasis added). In this embodiment, the microprocessor **22** has multiple outputs **23**, each one corresponding to a selectable stimulation level. The outputs **23** are converted by the pulse generator **24** into pulses **25** with a width that varies based on the selected stimulation level. Duncan, Fig. 2.

A preferred embodiment of the remote training system **10B** is illustrated in Figure 3. Duncan describes that embodiment by stating:

Microprocessor **22** supplies a signal **V18** on conductor **18** that includes a frequency-modulated stream of output pulses, all of the same pulse width, just as in the above described remote training system **10A** of FIG. 2. However, in FIG. 3 a filter circuit **39** including an integrator circuit **40** and an operational amplifier **42** filters the frequency-modulated stream of constant width pulses on conductor **18** to produce a drive signal **V25** on conductor **25**. Drive signal **25** includes pulses the widths of which correspond to the stimulus levels selected by switch **12** of remote transmitter **11**. Drive signal **V25** is applied to the gate of primary winding current switch MOSFET **30**, which operates as described above to control the durations of the currents in primary winding **31A**, and hence controls the amplitudes of the pulses of stimulation voltage V_o between skin-contacting electrodes **33** and **34**.

Duncan, Col. 5, lines 52-67 (emphasis added). In this preferred embodiment, the microprocessor **22** has a frequency-modulated output **V18** that is processed by a filter circuit **39**, which has an output of variable width pulses with the width related to the stimulation level. *Id.*

Independent Claim 1 and Dependent Claims 2-5

With respect to Claim 1, the Examiner states:

> As to claim 1, Duncan et al. discloses a 'transmitting unit (11) sending a coded signal inherently having an id code (it is inherent that remote control signals are coded so only the designated receiver of the signal processes the signals); a stimulation type code being a beep (51) or a shock (abstract) and a stimulation level code (shock intensity); a receiver (19); a processor (22); a speaker (51); a switch (claim 1); the processor controlling a pulse stream (fig. 8B) applied to the switch said pulse stream having a voltage level related to a value of the stimulation code; a transformer (31) electrically connected to the switch and producing a pulse stream (fig. 8B) and at least one electrode (33 and 34).

Paper Number 20050223, Application Serial No. 10/817,602, at 2-3 (emphasis added).

The Examiner asserts that Duncan discloses "the processor controlling a pulse stream (fig. 8B) applied to the switch said pulse stream having a voltage level related to a value of the stimulation code." Duncan states:

> Referring again to FIG. 3, microprocessor **22** provides a digital signal via conductor 48 to an encoded magnetic signal generator circuit **49**, the details of which are shown in FIG. 8. (An advantage to using a magnetic signal is that it is easy to comply with FCC regulations; however, a low power rf signal could be used instead.) Referring to FIG. 8, the magnetic encoder circuit **49** includes a transistor **49A** with its base connected to conductor **48**, its emitter connected to ground, and its collector connected to one terminal of an inductor **49B**, the other terminal of which is connected to +V. The encoded digital signal has the form indicated in FIG. 8B, in which a 4.5 millisecond burst of a 4 kilohertz squarewave followed by a 4 millisecond space representative of '1', and a 9 millisecond burst of the 4 kilohertz squarewave followed by the space represents a '0'."

Duncan, Col. 7, line 67, to Col. 8, line 4. The pulse stream to which the Examiner refers and illustrated in Figure 8B of Duncan is associated with a beeper **51** and is not the pulse stream in line with the switch **30**. *Id.*; Fig. 3. Accordingly, the Examiner has not shown that Duncan anticipates Claim 1.

Applicants respectfully submit that Duncan does not disclose the claim limitation of a "processor controlling a pulse stream applied to said switch, said pulse stream having a voltage level related to a value of said stimulation level code."

The pulse streams **V18** from the processor **22** are illustrated in Figure 5A of Duncan, and the pulse streams **V25** input to the switch **30** are illustrated in Figure

5B of Duncan. Duncan, Figs. 5A & 5B; Col. 6, line 54, to Col. 7, Line 28. Duncan states "The number of 10 microsecond pulses **44**, and hence the burst duration of t_{AMPL}, is determined by the present stimulus intensity setting of switch **12** on transmitter **11**." Duncan, Col. 6, lines 60-63. That is, the pulse train **V18** output from the processor **22** uses the number of pulses to correspond to the stimulus intensity.

A review of Figures 5A, 5B, and 5C shows that the pulse width of the Duncan device is related to the stimulation level code and to the pulse voltage from the output of the transformer. Two different pulse bursts **A**, **B** and **C**, **D** each having the same amplitude or voltage level, but varying in duration or width, are illustrated in Figure 5A as being output from the processor **22**. Duncan, Col. 6, lines 54-57.

Referring to Figure 5C, it is apparent that the wide widths **A**, **B** of the pulse burst **V18** and pulses **V25** result in a higher **Vo** than the narrower widths **C**, **D** of the pulse burst **V18** and pulses **V25**. Accordingly, Duncan discloses a pulse width related to the selected stimulation, which is not what is included in Claim 1. Further, Duncan does not disclose varying the voltage of the pulse bursts **V18** and/or the voltage of the pulses **V25** to control the voltage of the output of the transformer **Vo**.

It is respectfully submitted that Claim 1 is in condition for allowance because Duncan does not anticipate each and every limitation of the claim. Namely, Duncan does not disclose the processor producing a "pulse stream having a voltage level related to a value of said stimulation level code." Further, dependent Claims 2 to 5 are allowable for depending from an allowable base claim.

Dependent Claim 2

With respect to Claim 2, the Examiner states:

> As to claim 2, disclosed is a pulse stream having a fixed pulse width (fig. 8B), a fixed pulse frequency (fig. 8b) and a variable amplitude (fig. 8A).

Paper Number 20050223, Application Serial No. 10/817,602, at 3.

With respect to Figure 8A, Duncan states:

> FIG. 8A shows two noise waveforms **56** and **57** which could cause undesired digital signals to be input to microprocessor **51F** if the address supplied on conductor **48** were not encoded as described above. Noise waveform **56** is produced by transformer **31** when it produces stimulus signal **Vo**, and noise waveform **57** represents ambient random noise. Both noise waveforms can be filtered and/or shaped into digital error signals which appear on digital input of microprocessor **51F**. The use of magnetic signal **50** eliminates the use of a metal conductor between receiver circuit **19A** and beeper circuit **51**, and avoids a major reliability problem that would be caused by breakage of such a wire conductor.

Duncan, Col. 8, lines 36-48. Referring to Figures 3 and 8 of Duncan, which illustrate the components identified in the above quoted section, it is apparent that the waveforms illustrated in Figure 8A are not produced by the processor **22**.

With respect to Figure 8B, Duncan states:

> Referring to FIG. 8, the magnetic encoder circuit **49** includes a transistor **49A** with its base connected to conductor **48**, its emitter connected to ground, and its collector connected to one terminal of an inductor **49B**, the other terminal of which is connected to **+V**. The encoded digital signal has the form indicated in FIG. 8B, in which a 4.5 millisecond burst of a 4 kilohertz squarewave followed by a 4 millisecond space representative of "1", and a 9 millisecond burst of the 4 kilohertz squarewave followed by the space represents a "0".

Duncan, Col. 7, line 62, Col. 8, line 4. Referring to Figure 8 of Duncan, which illustrates the components identified in the above quoted section, it is apparent that the waveform illustrated in Figure 8B are not produced by the processor **22**.

Applicants recognize that depending upon where measurements are made in an electrical circuit, the measured waveforms vary. However, Claim 2 refers to the pulse stream controlled by the processor "applied to said switch," not processed by the beeper portion of the circuit.

Notwithstanding that Claim 2 is allowable for depending from an allowable base claim, the limitations of Claim 2 are not anticipated by Duncan because Duncan does not disclose a pulse stream from the processor **22** applied to the switch **30** that has a fixed width, fixed frequency, and a variable amplitude. Accordingly, Applicants respectfully request the Examiner withdraw his rejection to Claim 2.

Dependent Claim 3

With respect to Claim 3, the Examiner states:

> As to claim 3, disclosed is having a plurality of output connections that connect to a plurality of resistors that form a voltage divider network (fig. 3).

Paper Number 20050223, Application Serial No. 10/817,602, at 3.

A review of Figure 3 of Duncan does not illustrate a voltage divider network. No figure of Duncan illustrates a voltage divider network, particularly one connected to the output of the processor **22**. Claim 3 requires that the "processor [have] a plurality of output connections that connect to a plurality of resistors that form a voltage divider network connected to said switch." Figure 3 of Duncan illustrates a single output of the processor **22** connected to the filter **39**, which connects to the switch **30**.

Notwithstanding that Claim 3 is allowable for depending from an allowable base claim, the limitations of Claim 3 are not anticipated by Duncan because Duncan does not disclose a plurality of output connections that connect to a plurality of resistors that form a voltage divider network connected to said switch. Accordingly, Applicants respectfully request the Examiner withdraw his rejection to Claim 3.

Independent Claim 6

With respect to Claim 6, the Examiner states:

> As to claim 6, disclosed is a processor (22) that receives a coded signal, verifies the id code, and determines if a beep or shock is generated and generates the signal for a specified level (fig. 3); a switch (claim 1) controlled by the processor and the processor controlling the voltage level applied to the switch (table 1); a transformer producing a pulse having a pulse voltage directly related to said voltage level applied to said switch (fig. 8B); and at least one electrode (33 and 34) connected to the transformer.

Paper Number 20050223, Application Serial No. 10/817,602, at 3-4 (emphasis added).

Claim 6 includes the limitation for "a switch controlled by said processor, said processor controlling a voltage level applied to said switch." The Examiner points to Table 1 of Duncan in support of the rejection of Claim 6. However, Table 1 illustrates the correlation between the Selected Stimulation Intensity and the width of the pulse burst, t_{AMPLi}. As described above with respect to Claim 1 and as illustrated in Table 1,

Duncan uses pulse width to control the voltage of the shock applied to the animal. This is not the same as the claim limitation. Additionally, Figures 5A, 5B, and 5C of Duncan illustrate that the transformer pulse **Vo** has a voltage related to the width of the pulses **V25** applied to the switch **30**. Again, Duncan discloses something different than is claimed.

It is respectfully submitted that Claim 6 is in condition for allowance because Duncan does not anticipate each and every limitation of the claim. In particular, Duncan does not disclose the processor controlling the voltage level applied to the switch, nor does Duncan disclose the transformer pulse being directly related to the voltage level applied to the switch. Further, dependent Claim 7 is allowable for depending from an allowable base claim.

Independent Claim 8

With respect to Claim 8, the Examiner states:

> As to claim 8, disclosed is a processor (22) that receives a coded signal, verifies the id code, and determines if a beep or shock is generated and generates the signal for a specified level (fig. 3); a means for producing an electrical stimulation (24).

Paper Number 20050223, Application Serial No. 10/817,602, at 4.

Claim 8 includes a means-plus-function limitation, as defined by 35 U.S.C. § 112, sixth paragraph. A means-plus-function limitation must be interpreted to cover the corresponding structure, materials, or acts in the specification and "equivalents thereof." 35 U.S.C. § 112, sixth paragraph; *see also* MPEP § 2181. The Examiner "must apply 35 U.S.C. 112, sixth paragraph in appropriate cases, and give claims their broadest reasonable interpretation, **in light of and consistent with the written description of the invention in the application**." MPEP 2181, sub-section I, pg. 2100-220, 8th ed., rev. 2 (emphasis added).

In accordance with MPEP § 2181, it no longer is acceptable practice for the Examiner to interpret means-plus-function limitations "as reading on any prior art means or step which performed the function specified in the claim without regard for whether the prior art means or step was equivalent to the corresponding structure, material or acts described in the specification." MPEP § 2181, pg. 2100-220

(emphasis added). The current practice is that "the application of a prior art reference to a means or step plus function limitation requires that the prior art element perform the identical function specified in the claim." MPEP § 2182, pg. 2100-227. "However, if a prior art reference teaches identity of function to that specified in a claim, then under *Donaldson* **an examiner carries the initial burden of proof for showing that the prior art structure or step is the same as or equivalent to the structure, material, or acts described in the specification** which has been identified as corresponding to the claimed means or step plus function." *Id.* (emphasis added). The MPEP further states "The 'means or step plus function' limitation should be interpreted in a manner consistent with the specification disclosure." *Id.*

For making a *prima facie* case of equivalence for a means-plus-function limitation, the MPEP states

> If the examiner finds that a prior art element
>
> (A) performs the function specified in the claim,
> (B) is not excluded by any explicit definition provided in the specification for an equivalent, and
> (C) is an equivalent of the means-(or step-) plus-function limitation,
>
> the examiner should provide an explanation and rationale in the Office action as to why the prior art element is an equivalent.

MPEP § 2183, pg. 2100-228. With respect to the third element above, the prior art element is an equivalent, the MPEP states that a factor supporting such a conclusion is "(D) the prior art element is a structural equivalent of the corresponding element disclosed in the specification." MPEP § 2183, pg. 2100-228. The MPEP further requires that "the prior art element performs the function specified in the claim in substantially the same manner as the function is performed by the corresponding element described in the specification." MPEP § 2183, pg. 2100-228 (emphasis added).

Accordingly, it is necessary to consider the specification in determining the scope of the rejected claims. Claim 8 includes a limitation "means for producing an

electrical stimulation based on an output of said processor." Applicants' specification describes the circuit that produces the electrical stimulation based on the output of the processor **306**.

> **[0016]** Figure 4 is a schematic diagram of a portion of the receiver unit **104** showing only the relationship of the connections between the processor **306**, the switch **308**, and the transformer **310**. The processor **306** has four output connections **RB0**, **RB1**, **RB2**, **RB3** connected to the gate of single N-channel HEXFET power MOSFET **Q4**, which is the switch **308** illustrated in Figure 3. The drain of the MOSFET **Q4** is connected to the primary of the transformer **310**. The other end of the primary of the transformer **310** is connected to the power supply **V+**.
>
> * * *
>
> **[0018]** The output connections **RB0**, **RB1**, **RB2**, **RB3** of the controller **306** are bi-directional input/output (I/O) ports that can be programmed for internal weak pull-up. The output connections **RB0**, **RB1**, **RB2**, **RB3** are controlled to be in one of three states: ground; Vdd, which is the positive power supply voltage; or a high impedance, which is the same as an open circuit.
>
> **[0019]** The four output connections **RB0**, **RB1**, **RB2**, **RB3**, in combination with voltage divider resistors **R1**, **R2**, **R3**, **R4**, control the voltage applied to the gate of the MOSFET **Q4**. For example, driving output **RB3** to ground and the other outputs **RB0**, **RB1**, **RB2** to a high impedance or ground state causes the gate of the MOSFET **Q4** to be at the lowest possible voltage, ground, corresponding to a no stimulation level. Driving output **RB3** to Vdd and the other outputs **RB0**, **RB1**, **RB2** to a high impedance causes the gate of the MOSFET **Q4** to be at the highest possible voltage, corresponding to a high stimulation level. The gate voltage is set between these two extremes by setting the state of the outputs **RB0**, **RB1**, **RB2**, **RB3** such that the resistors **R1**, **R2**, **R3**, **R4** provide a voltage divider.

Specification, para. 16, 18, 19. Other portions of the Specification describe the pulse streams and waveforms related to the output of the processor **306** and the output of the transformer **310**. The above description is for a circuit substantially different than disclosed in Duncan, which does not disclose multiple outputs from the processor **22** going through a resistive network to the switch **30**.

Applicants respectfully submit that Claim 8 is not anticipated by Duncan because Duncan does not disclose any equivalent structures corresponding to those disclosed in Applicants' specification, and, therefore, Duncan does not teach every element of the claimed invention. In particular, Duncan does not disclose a resistive network connected to a plurality of processor outputs, with the resistive network

controlling the voltage of applied to the switch. Applicants respectfully submit that Claim 8 includes elements not disclosed by Duncan, and the Examiner has not provided a prima facie case showing that Duncan renders the claimed invention obvious. Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 8. Further, dependent Claims 9 and 10 are allowable for depending from an allowable base claim

Dependent Claim 9

With respect to Claim 9, the Examiner states:

> As to claim 9, disclosed is a pulse stream having a fixed pulse width (fig. 8B), a fixed pulse frequency (fig. 8b) and a voltage level (table 1).

Paper Number 20050223, Application Serial No. 10/817,602, at 4.

As discussed above with respect to Claim 2, Duncan does not disclose the processor **22** producing a pulse stream with "a fixed width, a fixed frequency, and a voltage level related to said specified stimulation level."

Notwithstanding that Claim 9 is allowable for depending from an allowable base claim, the limitations of Claim 9 are not anticipated by Duncan because Duncan does not disclose a pulse stream from the processor **22** applied to the switch **30** that has a fixed width, fixed frequency, and a voltage level related to said specified stimulation level . Accordingly, Applicants respectfully request the Examiner withdraw his rejection to Claim 9.

Independent Claim 11

With respect to Claim 11, the Examiner states:

> As to claim 11, disclosed is a receiver (19); a decoder (22); and a means for producing a shock (24).

Paper Number 20050223, Application Serial No. 10/817,602, at 4.

As discussed above with respect to Claim 8, Claim 11 includes means-plus-function limitations, which must be examined in light of the specification.

Additionally, Claim 11 includes the identical limitation as discussed above with respect to Claim 8. As noted in the discussion of Claim 8, Duncan does not disclose

Applicants respectfully submit that Claim 11 is not anticipated by Duncan because Duncan does not disclose any equivalent structures corresponding to those disclosed in Applicants' specification, and, therefore, Duncan does not teach every element of the claimed invention. In particular, Duncan does not disclose a means for producing an electrical stimulation based on said coded signal that includes a resistive network connected to a plurality of processor outputs, with the resistive network controlling the voltage of applied to the switch. Applicants respectfully submit that Claim 11 includes elements not disclosed by Duncan, and the Examiner has not provided a prima facie case showing that Duncan renders the claimed invention obvious. Accordingly, Applicants respectfully request that the Examiner withdraw his rejection of Claim 11. Further, dependent Claims 12 and 13 are allowable for depending from an allowable base claim.

Dependent Claim 12

With respect to Claim 12, the Examiner states:

> As to claim 12, disclosed is a pulse stream having a fixed pulse width (fig. 8B), a fixed pulse frequency (fig. 8b) and a voltage level (table 1).

Paper Number 20050223, Application Serial No. 10/817,602, at 4.

As discussed above with respect to Claim 2, Duncan does not disclose the processor **22** producing a pulse stream with "a fixed width, a fixed frequency, and a voltage level related to said specified stimulation level."

Notwithstanding that Claim 12 is allowable for depending from an allowable base claim, the limitations of Claim 9 are not anticipated by Duncan because Duncan does not disclose a pulse stream from the processor **22** applied to the switch **30** that has a fixed width, fixed frequency, and a voltage level related to said specified stimulation level . Accordingly, Applicants respectfully request the Examiner withdraw his rejection to Claim 12.

Claims 14-28

With respect to Claims 14-28, the Examiner states:

> As to claims 14-28, the method steps of the instant claim are readily apparent during the operation of the device of Duncan et al.

Paper Number 20050223, Application Serial No. 10/817,602, at 5.

Initially, Applicants note that the Examiner has provided an omnibus rejection. The MPEP provides guidance to examiners in rejecting claims. In particular, the MPEP states that omnibus rejections should be avoided. MPEP § 707(d), at 700-113, 8th ed., rev. 1. Further, the MPEP states: "A plurality of claims should never be grouped together in a common rejection, unless that rejection is equally applicable to all claims in the group." *Id.* This is in keeping with the goal of examination, which is "to clearly articulate any rejection early in the prosecution process so that the applicant has the opportunity to provide evidence of patentability and otherwise reply completely at the earliest opportunity." MPEP § 706, at 700-17.

Contrary to the above requirements, the Examiner has rejected Claims 14-28 without addressing the unique limitations of each claim. Applicants remind the Examiner that in order to support a rejection, each and every limitation of each claim must be found, either expressly or inherently, in the prior art. *See* MPEP 2131 and 2143. Applicants respectfully submit that the Examiner has not addressed each claim and each element and limitation of each claim as required by the MPEP. Accordingly, it is respectfully requested that the Examiner withdraw the rejections or, in the alternative, address each claim and each element as required. In the latter case, because such restatement of the rejection is necessary to complete the statement of the grounds for rejection (see MPEP 706.07), it is respectfully submitted that it would be inappropriate to make the next Examiner's action final, unless, of course, the next action is a Notice of Allowance.

Notwithstanding the above concerns and in an attempt to anticipate the Examiner's complete statement of the grounds for rejection, Applicants herein address the rejected claims and identify at least one element and/or limitation not found in the prior art, as appropriate.

Claims 14-16

With respect to independent Claim 14, one limitation is that the software process includes "outputting said control signal to produce a signal having a voltage corresponding to said stimulation level code." As noted above, Duncan discloses a device with a processor programmed to output a pulse burst of variable width and with a constant voltage. Duncan, Figs. 5A, 5B, 5C. Claim 14 requires that the control signal output from the processor produce a signal with a voltage corresponding to the stimulation level code.

Applicants respectfully submit that Duncan does not anticipate Claim 14 because at least one claim limitation is not disclosed in Duncan. In particular, the processor **22** disclosed in Duncan controls the pulse burst width to produce the desired stimulation level and Duncan does not disclose the processor **22** producing a signal that varies the voltage to produce the desired stimulation level. Accordingly, Applicants respectfully request the Examiner withdraw the rejection to Claim 14. Further, dependent Claims 15 and 16 are allowable for depending from an allowable base claim.

Claims 17-20

With respect to independent Claim 17, Applicants have amended the claim to clarify that the voltage level corresponding to said stimulation level code is the voltage level as controlled by the processor and applied to the switch, and not the electrical stimulation signal applied to the animal. This amendment is made to distinguish the invention of Claim 17 from Duncan, which does not disclose the processor **22** producing a signal with a variable voltage that is applied to the switch **30**.

Additionally, Claim 20 has been amended to correct reflect the antecedent basis for the electrical stimulation signal. The amendment to Claim 20 does not change the scope of the claim.

Accordingly, Applicants respectfully request the Examiner withdraw the rejection to Claim 17. Further, dependent Claims 18-20 are allowable for depending from an allowable base claim.

Claims 21-24

With respect to independent Claim 21, two limitations are the step of "c2) generating an input pulse stream having a fixed pulse width, a fixed frequency, and a pulse voltage equal to said voltage level" and the step of "c3) applying said input pulse stream to an output pulse generator." As noted above, Duncan discloses a device with a processor **22** programmed to output a pulse burst of variable width and with a constant voltage. Duncan, Figs. 5A, 5B, 5C. Claim 21 requires that the input pulse stream **V18** produce a signal with a voltage corresponding to the stimulation level code and that this input pulse stream be the signal before the output pulse generator.

Applicants respectfully submit that Duncan does not anticipate Claim 21 because at least one claim limitation is not disclosed in Duncan. In particular, the processor **22** disclosed in Duncan controls the pulse burst width to produce the desired stimulation level and Duncan does not disclose the processor **22** producing a signal that varies the voltage to produce the desired stimulation level. Accordingly, Applicants respectfully request the Examiner withdraw the rejection to Claim 21. Further, dependent Claims 22-24 are allowable for depending from an allowable base claim.

Claims 25-28

With respect to independent Claim 25, two limitations are the step of "b1) determining a voltage level corresponding to said stimulation level code" and the step of "b2) applying to a switch an input pulse stream having a fixed pulse width, a fixed frequency, and a pulse voltage equal to said voltage level." As noted above, Duncan discloses a device with a processor **22** programmed to output a pulse burst **V18** of variable width and with a constant voltage. Duncan, Figs. 5A, 5B, 5C. Claim 25 requires that the input pulse stream have a fixed pulse width, a fixed frequency, and a pulse voltage equal to said voltage level and this input pulse stream be applied to a switch.

Applicants respectfully submit that Duncan does not anticipate Claim 25 because at least one claim limitation is not disclosed in Duncan. In particular, the processor **22** disclosed in Duncan controls the pulse burst width to produce the desired stimulation level and Duncan does not disclose the processor **22** producing a

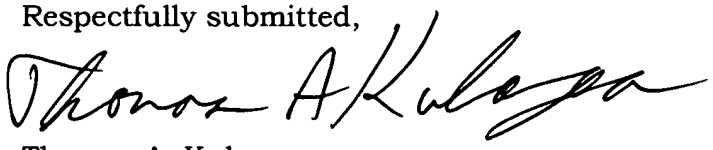
signal that varies the voltage to produce the desired stimulation level. Accordingly, Applicants respectfully request the Examiner withdraw the rejection to Claim 25. Further, dependent Claims 26-28 are allowable for depending from an allowable base claim.

Conclusion

In view of the amendment of Claims 15, 16, 17, and 20, it is believed that the above-identified patent application is in a condition for the issuance of a Notice of Allowance. Such action by the Examiner is respectfully requested. If, however, the Examiner is of the opinion that any of the drawings or other portions of the application are still not allowable, it will be appreciated if the Examiner will telephone the undersigned to expedite the prosecution of the application.

Please charge any additional fees associated with this communication, or credit any overpayment, to Deposit Account No. 16-1910 (29106.00).

Respectfully submitted,



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